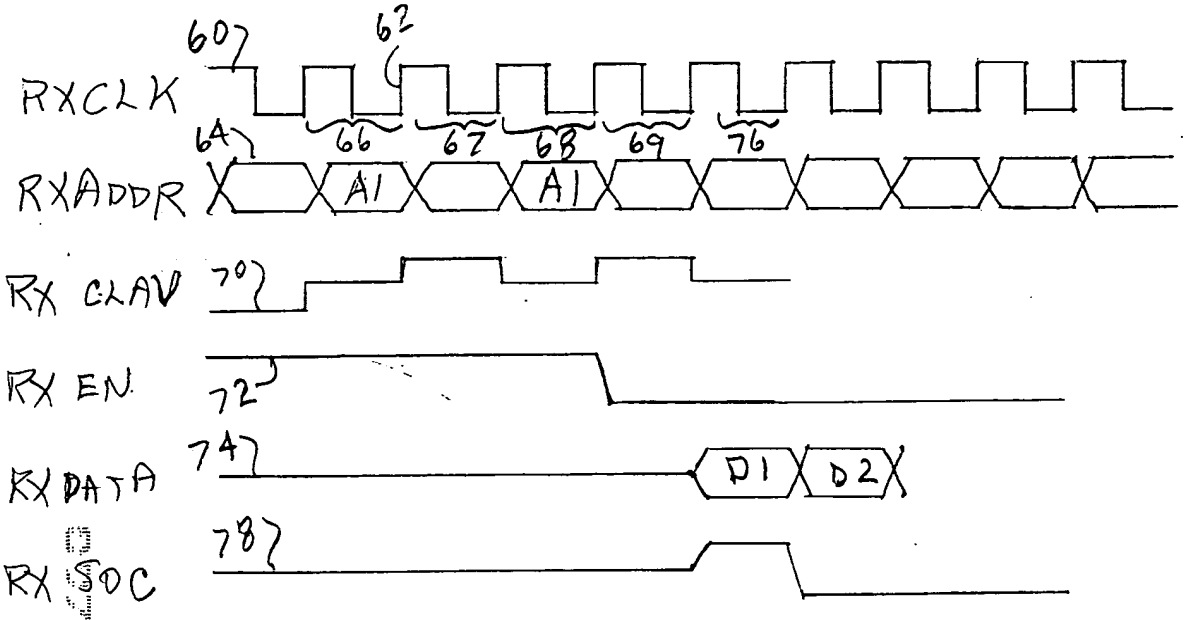
60
62
RXCLK
64
66
67
68
69
70
RXADDR
A1
A1
RX CLAV
RX EN
72
RX DATA
74
D1
D2
RX SOC
78

FIGURE 2

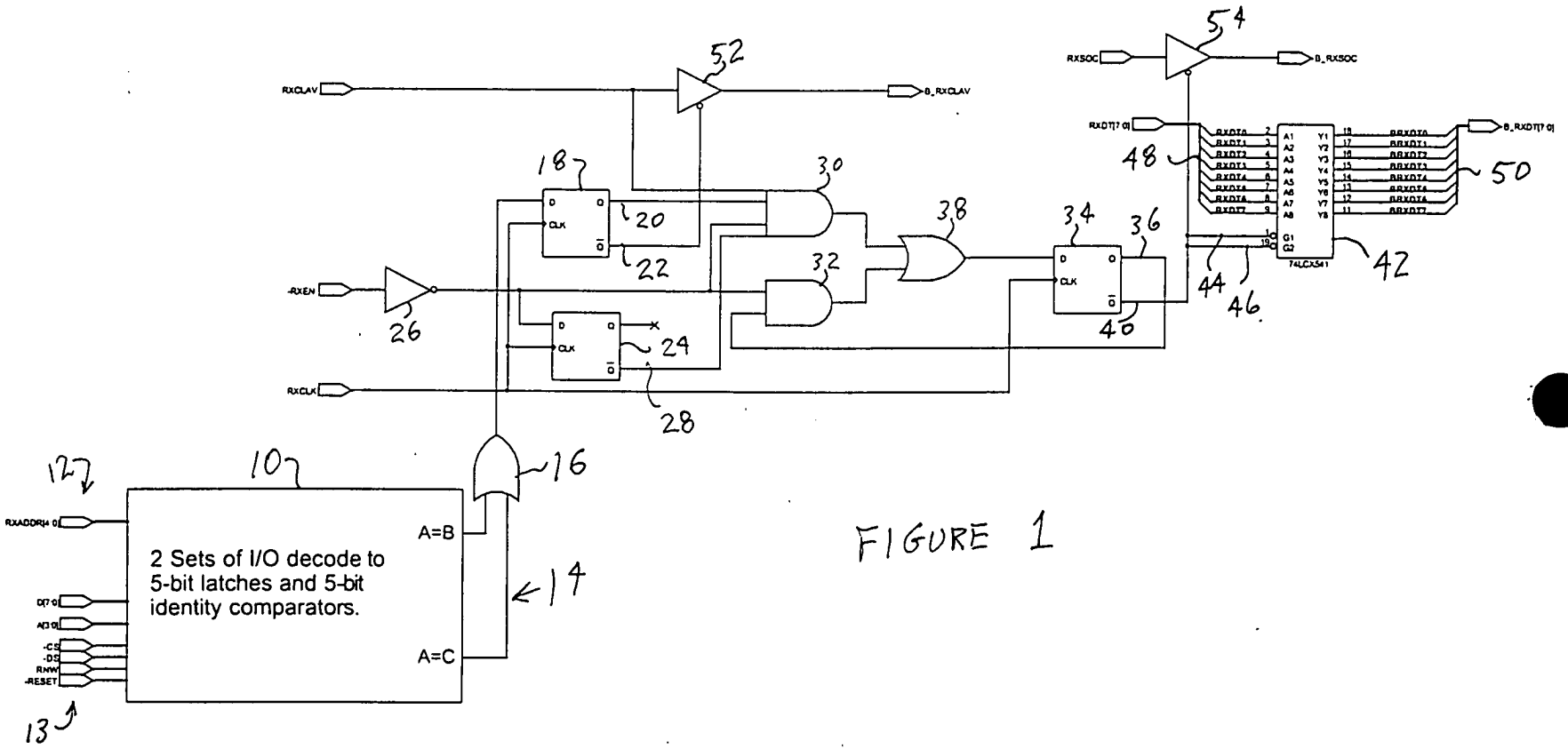
RXCLAV
B_RXCLAV
52
54
RXSOC
B_RXSOC
RXDT[7:0]
B_RXDT[7:0]
48
50
18
20
22
30
32
38
34
36
40
44
46
42
74LCX541
-RXEN
26
24
RXCLK
28
16
12
10
14
RXADDR[4:0]
D[7:0]
A[3:0]
-CS
-DS
RNW
-RESET
A=B
A=C
2 Sets of I/O decode to 5-bit latches and 5-bit identity comparators.
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FIGURE 1